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PATENT APPLICATION
Docket No. 15436.330.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of		)
	Gerald L. Dybsetter et al.	)
Serial No.:	10/814,392	) Art Unit) 2185
Filed:	March 31, 2004	)
For:	CONTINGENT PROCESSOR TIME DIVISION MULTIPLE ACCESS OF MEMORY IN A MULTI-PROCESSOR SYSTEM TO ALLOW SUPPLEMENTAL MEMORY CONSUMER ACCESS	)
Confirmation No.:	5366	)
Customer No.:	022913	)
Examiner:	Yaima Campos	)

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MAIL STOP: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In reply to the Final Office Action mailed January 10, 2007 (the "Final Office Action"), Applicants respectfully request a panel review of the final rejection under 35 U.S.C. § 103(a) discussed in the remarks below. No amendments are being filed with this Request. This Request is being filed concurrently with a Notice of Appeal.

Claims 1-6 and 9-33 have been finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,401,176 to Fadavi-Ardekani et al. ("*Fadavi-Ardekani*") in view of U.S. Patent No. 5,893,153 to Tzeng et al. ("*Tzeng*"). Claims 7-8 have been finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fadavi-Ardekani* and *Tzeng* and further in view of U.S. Patent No. 6,275,885 to Chin et al. ("Chin"). The Examiner has also rejected claims 34-42 under 35 U.S.C. § 103(a) as being unpatentable over *Fadavi-Ardekani* and *Tzeng* and further in view of assertions by the Examiner that it would have been obvious to use the controller as claimed in these claims.

Legal and Factual Deficiencies

1. Failure to Demonstrate that the Cited References Teach or Suggest All Claim Limitations

In the Final Office Action, the Examiner has failed to establish that the cited references, either alone or in combination, teach or suggest all the claim limitations of the rejected claims.

For example, each of the rejected independent claims 1, 20, and 28 require that a "memory controller" perform or be configured to perform:

> "an act of [] allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles."

(hereinafter the "guaranteed access" limitation) *(Emphasis added)*.

As outlined in Applicant's Paper filed October 30, 2006, Applicants understand that the Examiner has characterized an "arbiter [102/202]" of *Fadavi-Ardekani* as corresponding to the "memory controller," a "super agent A" of *Fadavi-Ardekani* as corresponding to the "first processor," and a "shared synchronous memory 200" of *Fadavi-Ardekani* as corresponding to the "system memory" recited in the claims. *See Final Office Action, pages 2-3*. In asserting that *Fadavi-Ardekani* discloses the above cited requirement of claims 1, 20, and 28, the Examiner has stated that "the 'super agent' is not required to arbitrate for access to memory with the other agents (Column 5, lines 30-38); therefore, the 'super agent' is guaranteed access to memory." *Final Office Action, page 3.*

In light of the foregoing, it thus appears to be the position of the Examiner that *Fadavi-Ardekani* discloses that the arbiter 102/202 performs or is configured to perform "an act of [] allotting a first division of each of a plurality of memory access cycles" for the "super agent A."

Despite the assertions of the Examiner, however, it is apparent from Figure 3 of *Fadavi-Ardekani* that any division of "memory access cycles" allotted and guaranteed to the "super agent A" are not allotted and guaranteed by the arbiter 202. *Fadavi-Ardekani* confirms this understanding, stating:

> [I]t is within the principles of the present invention as will be discussed in more detail herein below to designate one of the plurality of agents as a super agent and allow that super agent to communicate with the shared synchronous memory 200 without requiring that super agent to arbitrate for ownership of the shared synchronous memory 200. In this case, all other agents would monitor the super agent's communications with the shared synchronous memory 200.
>
> For instance, FIG. 3 shows a plurality of agents including a super agent A and a non-super agent B wherein the super agent A is allowed to communicate with the shared synchronous memory 200 *without* arbitration.
>
> In particular, FIG. 3 shows a shared synchronous memory 200 which is accessible by both a super agent A and a non-super agent B. The super agent A has direct access to the shared synchronous memory 200, while the non-super agent B accesses the

> shared synchronous memory 200 under the control of an arbiter and switch [202]. Thus, the super agent A obtains access to the shared synchronous memory 200 directly via a communication path 220, while the non-super agent B requests access to the shared synchronous memory 200 via the arbiter and switch 202 using communication paths 222a, 222b and 222c.

Column 5, lines 26-49 (emphasis added).

As argued in Applicant's Paper filed October 30, 2006, in light of the disclosure of *Fadavi-Ardekani* that "The super agent A has direct access to the shared synchronous memory 200, while the non-super agent B accesses the shared synchronous memory 200 under the control of an arbiter and switch [202]," that reference appears to contradict the assertion of the Examiner that the arbiter 202 can be characterized as "allotting a first division of each of a plurality of memory access cycles memory access cycles" to the super agent A, since it is clear that the super agent A is not "under the control of an arbiter and switch [202]" as the Examiner appears to allege. See, *column 5, lines 41-44 (emphasis added)*.

In the Final Office Action, the Examiner has responded to this argument by combining the teachings of Column 8, lines 49-57 of *Fadavi-Ardekani* with the teachings of Column 4, lines 45-48 of *Fadavi-Ardekani* and by asserting "therefore, the arbiter is used to encode a priority level to an agent, making this agent a 'super agent' such that 'memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles' as claimed by Applicant." *See Final Office Action, pages 13-14*. Despite this assertion by the Examiner, it is clear from the context of these citations that the first citation makes reference to the embodiment of Figure 3 of *Fadavi-Ardekani* and the second citation makes reference to the embodiment of Figure 2 of *Fadavi-Ardekani*. Given that the Examiner has made no attempt to demonstrate a suggestion or motivation to modify these embodiments, a reasonable expectation of success in such a modification, nor that such a modification would include teach or suggest all the claim limitations, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to each of claims 1, 20, and 28.

In the Final Office Action, the Examiner has also responded to the above-recited argument by citing broadly to Figure 9 and the related description in *Fadavi-Ardekani* and by asserting that Figure 9 and the related description disclose the "guaranteed access" limitation. *See Final Office Action, pages 14-15.* However, this broad citation to Figure 9 and to the related description fails to identify, with any specificity whatsoever, which element of Figure 9 is purported by the Examiner to constitute, for example, the "first processor" or "that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles" as recited in each of the rejected independent claims. At least because the Examiner has failed to demonstrate that this limitation is taught in *Fadavi-*

Ardekani, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to each of claims 1, 20, and 28.

The rejection of independent claims 1, 20, and 28 is problematic for other reasons as well. For example, each of the currently pending independent claims 1, 20, and 28 require "a system memory…[and] a plurality of processors…that each accesses the system memory through a memory controller" (hereinafter the "through a memory controller" limitation). *(Emphasis added)*. The Examiner has alleged that "Fadavi-Ardekani discloses…a system memory…a plurality of processors…that each access the system memory through a memory controller." *Final Office Action, pages 2-3 (emphasis added)*.

As argued in Applicant's Paper filed October 30, 2006, however, Applicants respectfully note that Figure 3 and the portions of *Fadavi-Ardekani* cited above clearly disclose that "the super agent A obtains access to the shared synchronous memory 200 directly via a communication path 220," and not through the arbiter 202 (characterized by the Examiner as corresponding to the claimed "memory controller"). *Column 5, lines 44-46 (emphasis added)*.

In the Final Office Action, the Examiner has responded to this argument by citing broadly to Figure 9 and the related description in *Fadavi-Ardekani* and by asserting that Figure 9 and the related description disclose the "through a memory controller" limitation. *See Final Office Action, pages 15-16.* Despite this assertion by the Examiner, as discussed above, this broad citation to Figure 9 and to the related description fails to identify, with any specificity whatsoever, which element of Figure 9 is purported by the Examiner to constitute, for example, the "first processor" or "that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles" as recited in claims 1, 20, and 28. At least because the Examiner has failed to demonstrate that this limitation is taught in *Fadavi-Ardekani*, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with respect to each of claims 1, 20, and 28.

As the foregoing makes clear, the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 1, 20, and 28, at least because the Examiner has failed to establish that *Fadavi-Ardekani* and *Tzeng*, either alone or in combination, teach or suggest all the claim limitations of claims 1, 20, and 28. Applicants thus respectfully submit that the rejection of claims 1, 20, and 28, as well as the rejection of corresponding dependent claims 2-19, 21-27 and 29-42, should be withdrawn.

2. Conclusion

In light of the discussion set forth herein, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 1-42, at least because even if

the references are combined as the Examiner has suggested would be obvious to do, the Examiner has failed to establish that the references when combined include all the limitations of the rejected claims.

Because the rejections set forth in the Final Office Action include a variety of legal and factual deficiencies, Applicants are entitled to a pre-appeal brief review of the Final Office Action. Moreover, in view of the foregoing remarks, Applicants respectfully request withdrawal of finality of the rejection, reconsideration and reexamination of this application, and the timely allowance of the pending claims.

Dated this 2rd day of July, 2007

Respectfully submitted,

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